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Title:

METHOD OF REFRESHING A PCRAM MEMORY DEVICE

Inventors:

John T. Moore, Terry L. Gilton, and Kristy A. Campbell

Thomas J. D'Amico
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700

METHOD OF REFRESHING A PCRAM MEMORY DEVICE

FIELD OF THE INVENTION

[0001] The invention relates generally to the field of semiconductor devices and, more particularly, to programmable conductor random access memory (PCRAM) devices.

BACKGROUND OF THE INVENTION

[0002] Microprocessor-controlled integrated circuits are used in a wide variety of applications. Such applications include, for example, personal computers, vehicle control systems, telephone networks, and a host of consumer products. As is well known, microprocessors are essentially generic devices that perform specific functions under the control of a software program. This program is stored in one or more memory devices that are coupled to the microprocessor. Not only does the microprocessor access memory devices to retrieve the program instructions, but it also stores and retrieves data created during execution of the program in one or more memory devices.

[0003] There are a variety of different memory devices available for use in microprocessor-based systems. The type of memory device chosen for a specific function within a microprocessor-based system depends largely upon what features of the memory are best suited to perform the particular function. For instance, random access memories such as dynamic random access memories (DRAMs) and static

random access memories (SRAMs) are used to temporarily store program information and data "actively" being used by the microprocessor. The data stored in random access memories may be read, erased, and rewritten many times during the execution of a program or function. Read only memories (ROMs), "write once read many" devices (WORMs) and electrically erasable programmable read only memories (EEPROMs), and flash memories on the other hand, are used as long term memory devices which permanently store information about the microprocesor system or store software programs or instructions for performing specific functions until erased or deleted by a user, for example.

[0004] Random access memories tend to provide greater storage capability and programming options and cycles than read only memories, but they must be continually powered in order to retain their content. Most random access memories store data in the form of charged and discharged capacitors contained in an array of memory cells. Such memory cells, however, are volatile in that the stored charges will dissipate after a relatively short period of time because of the natural tendency of an electrical charge to distribute itself into a lower energy state. For this reason, most random access memories such as DRAMs must be refreshed, that is, the stored value must be rewritten to the cells, about every 100 milliseconds in order to retain the stored data in the memory cells. Even SRAMs, which do not require refreshing, will only retain stored data as long as power is supplied to the memory device. When the power supply to the memory device is turned off, the data is lost.

[0005] Read only memories presently used in microprocessor devices are non-volatile, that is, capable of retaining stored information even when power to the memory device is turned off. Some read only memory devices are constructed so that once programmed with data, they cannot be reprogrammed. The read only memories

that can be reprogrammed have complex structures which are difficult to manufacture, occupy a large amount of space and consume large quantities of power. For these reasons, read only memories are unsuitable for use in portable devices and/or as substitutes for the frequently accessed random access memories, i.e., memories capable of 10^{14} programming cycles or more.

[0006] Efforts have been underway to create a commercially viable memory device that is both randomly accessed and nonvolatile. To this end, various implementations of such nonvolatile random access memory devices are presently being developed which store data in a plurality of memory cells by structurally or chemically changing the resistance across the memory cells in response to predetermined voltages respectively applied to the memory cells. Examples of such variable resistance memory devices include memories using variable resistance polymers, perovskite, doped amorphous silicon or doped chalcogenide glass.

[0007] In a variable resistance memory cell, a first value may be written thereto by applying a voltage having a predetermined level to the memory cell, which changes the electrical resistance through the memory cell relative to the condition of the memory cell prior to the application of the voltage. A second value, or the default value, may be written to or restored in the memory cell by applying a second voltage to the memory cell, to thereby change the resistance through the memory cell back to the original level. The second voltage is in the negative direction of the first voltage and may or may not have the same magnitude as the first voltage. Each resistance state is stable, so that the memory cells are capable of retaining their stored values without being frequently refreshed. In this regard, since the variable resistance materials can be "programmed" to any of the stable resistance values, such variable resistance memory cells are known as programmable conductor random access memory (PCRAM) cells.

[0008] The value of the PCRAM cell is read or "accessed" by applying a read voltage to determine the resistance level across the cell. The magnitude of the read voltage is lower than the magnitude of the voltage required to change the resistance of the PCRAM cell. In a binary PCRAM cell, upon determining the resistance level of the PCRAM cell, the detected resistance level is compared with a reference resistance level. Generally, if the detected resistance level is greater than the reference level, the memory cell is determined to be in the "off" state, or storing, for example, a value of "0." On the other hand, if the detected resistance level is less than the reference level, the memory cell is determined to be in the "on" state, or storing, for example, a value of "1."

[0009] FIG. 1 generally shows a basic composition of a PCRAM cell 10 constructed over a substrate 12, having a variable resistance material 16 formed between two electrodes 14, 18. One type of variable resistance material may be amorphous silicon doped with V, Co, Ni, Pd, Fe and Mn as disclosed in U.S. Patent No. 5,541,869 to Rose et al. Another type of variable resistance material may include perovskite materials such as $Pr_{1-x}Ca_xMnO_3$ (PCMO), $La_{1-x}Ca_xMnO_3$ (LCMO), $LaSrMnO_3$ (LSMO), $GdBaCo_xO_y$ (GBCO) as disclosed in U.S. Patent No. 6,473,332 to Ignatiev et al. Still another type of variable resistance material may be a doped chalcogenide glass of the formula A_xB_y, where "B" is selected from among S, Se and Te and mixtures thereof, and where "A" includes at least one element from Group IIIA (B, Al, Ga, In, Tl), Group IVA (C, Si, Ge, Sn, Pb), Group VA (N, P, As, Sb, Bi), or Group VIIA (F, Cl, Br, I, At) of the periodic table, and with the dopant being selected from among the noble metals and transition metals, including Ag, Au, Pt, Cu, Cd, Ir, Ru, Co, Cr, Mn or Ni, as disclosed in U.S. Published Application Nos. 2003/0045054 and 2003/0047765 to Campbell et al. and Campbell, respectively. Yet another type of variable resistance material includes a carbon-polymer film comprising carbon black particulates or graphite, for example, mixed into a plastic polymer, such as that disclosed in U.S. Patent No. 6,072,716 to

Jacobson et al. The material used to form the electrodes 14, 18 can be selected from a variety of conductive materials, such as tungsten, nickel, tantalum, titanium, titanium nitride, aluminum, platinum, or silver, among others.

[0010] In FIG. 2, a PCRAM cell 100 is shown to include an access device 102, a programmable conductor memory element 104, and a cell plate 110. The access device 102 is a transistor having a gate 102a coupled to a word line 106 and one terminal (source) 102b coupled to a bit line 108. The other terminal (drain) 102c of the access device 102 is coupled to one end of the programmable conductor memory element 104, while the other end of the programmable conductor memory element 104 is coupled to the cell plate 110. The cell plate 110 may span and be coupled to several other PCRAM cells, and may form the anode of all the memory elements 104 in an array of PCRAM cells. The cell plate 110 is also coupled to a potential source 112.

[0011] A representative diagram of the physical structure of the memory cell 100 is shown in FIG. 3. In particular, an n-doped substrate 126 includes a p-doped region 124. Two n-wells 120, 122 are formed in the p-doped region 124. Access device 102 is formed on the surface of the substrate 126 between the two n-wells 120, 122, so that the two n-wells 120, 122 serve as the source 102b and drain 102c, respectively, of the access device 102. Word line 106 is formed as a conductive strip extending into the page across the top of access device 102. Bit line 108 is connected directly to the n-well 120 forming the source 102b of the access device 102. Programmable conductor memory element 104 is formed on the substrate with its cathode 114 in contact with n-well 122 and the cell plate 110 (only a portion of which is shown) as its anode. The cell plate 110 of memory element 104 is connected to a potential source 112.

[0012] In the conventional operating scheme, when the memory element 104 is idle, the voltage across the anode 110 and the cathode 114 is 0 V. In order to perform

any access operations including programming the programmable conductor memory element 104 to the low resistance state, erasing a programmed memory element (*i.e.*, returning the memory element to the high resistance state), or reading the value stored in memory element 104, the word line 106 must be activated by applying a threshold voltage V_G. The activated word line which closes the gate 102a of the access device 102 so that an n-channel is formed in the substrate 126 under the gate structure of access device 102 and across the gap between the two n-wells 120, 122 to activate the device 102 . Upon activating the access device 102, the memory element 104 can be programmed to the low resistance state by applying a write (positive) voltage having at least the magnitude of a threshold voltage V_T across the memory element 104.

[0013] Application of the write voltage may be achieved by raising the potential at the cell plate 110 (anode) relative to the access device drain 102b by applying or raising the voltage at the potential source 112, lowering the potential of the bit line 108, or a combination of both. To erase a programmed memory element 104, a negative voltage having a magnitude of at least a threshold erase voltage is applied between the anode and the cathode of the memory element 104, such that the potential at the potential source 112 is lower than the potential of the bit line 108.

[0014] The value stored in the memory element 104 can be read by applying a positive voltage, either by raising the potential at the anode or lowering the potential of the bit line 108 or both, which is less than the voltage level required to program the memory element to the low resistance state.

[0015] In a bistable PCRAM cell, the programmable conductor memory element 104 stores, for example, a binary 0 when in a high resistance state, and a binary 1 when in the low resistance state. The memory element 104 is ideally programmed to the low resistance state, *e.g.*, to store a binary 1, by applying a positive voltage having a

magnitude at least that of a threshold write voltage, and can be restored to the high resistance state, *e.g.*, to store a binary 0, by applying a negative voltage having a magnitude of at least a threshold erase voltage. Of course, the values "0" and "1" relative to the high and low resistance state, respectively, are user-defined, and thus could be reversed, with the high resistance state representing the value "1" and the low resistance state representing the value "0." The memory element can be nondestructively read by applying a reading voltage having a magnitude of less than the threshold write voltage.

[0016] As with volatile RAMs, PCRAMs are arranged as an array of memory cells and are written, erased, and read using a controller. FIG. 4 illustrates a memory device 200 comprising an array of memory cells arranged by tiling a plurality of memory cells 100a-100f together so that the memory cells along any given bit line 108a, 108b do not share a common word line 106a-106c. Conversely, the memory cells 100a-100f along any word line 106a-106c do not share a common bit line 108a-108b. In this manner, each memory cell is uniquely identified by the combined selection of the word line to which the gate of the memory cell access device is connected, and the bit line to which the drain of the memory cell access device is connected.

[0017] Each word line 106a-106c is connected to a word line driver 202a-202c via a respective transistor 204a-204c for selecting the respective word line for an access operation. The gates of the transistors 204a-204c are used to selectively couple/decouple the word lines 106a-106c to/from the word line drivers 202a-202c. Similarly, each bit line 108a-108b is coupled to a driver 206a-206b via selector gates 208a-208b. The current and/or resistance of a selected memory cell 100a-100f is measured by sensor amplifiers 210a-210b connected respectively to the bit lines 108a-108b.

[0018] For simplicity, FIG. 4 illustrates a memory array having only two rows of memory cells 100 on two bit lines 108a-108b and three columns of memory cells 100 on three word lines 106a-106c. However, it should be understood that in practical applications, memory devices would have significantly more cells in an array. For example, an actual memory device may include several million cells 100 arranged in a number of subarrays.

[0019] While the overall operating scheme of the memory device 200 may be similar regardless of the type of variable resistance material used in the memory elements, much research of late has focused on memory devices using memory elements having doped chalcogenide materials as the variable resistance material. More specifically, memory cells having a variable resistance material formed of germanium-selenide glass having a stoichiometry of Ge_xSe_{100-x}, with x ranging from about 20 to about 43, have been shown to be particularly promising for providing a viable commercial alternative to traditional DRAMs.

[0020] Generally, a chalcogenide PCRAM cell having such stoichiometry has an initial and "off" state resistance of over 100 K Ω (*e.g.*, 1 M Ω). To perform a write operation on a chalcogenide memory cell in its normal high resistive state, a voltage having at least a threshold potential is applied to the electrode serving as the anode, with the cathode held at the reference potential or ground. Upon applying the threshold level voltage, *i.e.*, a write voltage, the resistance across the memory cell changes to a level dramatically reduced from the resistance in its normal state, to a resistance less than 100 K Ω (*e.g.*, 20 K Ω), whereupon the cell is considered to be in the "on" state.

[0021] The PCRAM cell retains this new lower level of resistivity until the resistivity is changed by another qualifying voltage level applied to one of the

electrodes of the cell. For example, the memory cell is returned to the high resistance state by applying an erase voltage thereto in the negative direction of the voltage applied in the write operation (to achieve the lower resistance state). The erase voltage may or may not be the same magnitude as the write voltage, but is at least of the same order of magnitude.

[0022] Although it is not clearly understood what change or changes are induced in the doped chalcogenide material by the application of the threshold potential to result in the stable low resistant state, it is believed that the metal ions incorporated into the chalcogenide material somehow become aligned into a low resistance conductive configuration between the electrodes once the applied voltage reaches the threshold level. At least two theories exist as to the precise nature of the alignment.

[0023] In one theory, the metal ions within the chalcogenide material begin to plate on the cathode and progress through the chalcogenide material toward the anode upon the application of the threshold voltage level of a write operation. The metal ions continue to agglomerate until a conductive dendrite or filament is extended between the electrodes to thereby interconnect the top and bottom electrodes to create an electrical short circuit. Upon application of the negative threshold voltage, the dendrite recedes from the anode as the metal ions return to solution in the chalcogenide material or return to the source layer.

[0024] In a second theory, when an initial write signal having a threshold positive voltage level is applied to the memory cell, at least one conductive channel is formed in the chalcogenide material, and the metal ions are caused to agglomerate along the channels(s), thereby lowering the electrical resistance across the cell. Upon application of an erase signal having a negative threshold voltage level to the cell, the

conductive channel(s) remain in place, but the metal ions are caused to move away from the conductive channel(s), thereby raising the electrical resistance across the cell. Subsequent write signals cause the metal ions to re-agglomerate along the channel(s). The resistance through the cell in the write and erase states is thus determined by the amount of metal ions agglomerated along the channel(s).

[0025] When written to the low resistance state, chalcogenide PCRAM cells can retain this state for several hours, days, even weeks. In this regard, such PCRAM devices are relatively non-volatile as compared to DRAM devices. However, while chalcogenide PCRAM cells in the high resistance state are completely non-volatile, PCRAM cells written to the low resistance state will gradually lose their conductivity across the chalcogenide glass layer and drift towards the high resistance state after an extended period of time. In particular, it has been found that such chalcogenide PCRAM devices which are written according to high speed algorithms, *i.e.*, using write voltages each having a pulse width of less than 100 ns, have a tendency to gradually lose their low resistance characteristic over time, *e.g.*, a week. It is desirable to use such high speed algorithms to write PCRAM devices to accommodate the demands of current operating speeds in state-of-the-art processors. Accordingly, PCRAM memory devices operated using high speed algorithms should be intermittently refreshed to maintain optimal operation of the PCRAM memory devices.

[0026] Refresh operations are well known in DRAM devices. Specifically, in DRAM devices memory cells must be refreshed frequently, *e.g.*, every 100 milliseconds, and regardless of the value stored in each cell. Additionally, DRAM cells are refreshed with every read operation. PCRAM cells, on the other hand, only require refreshing on a much more sporadic basis, *e.g.*, once every several days to once per week. Moreover, only PCRAM cells written to the low resistance state need periodic refreshing, since

PCRAM cells in the high resistance state are not at risk of losing their stored values. One feature resulting from these characteristics of PCRAM devices is that PCRAM devices do not require the dedicated circuitry necessary in DRAM devices to perform the refresh operations.

[0027] U.S. Application Serial No. 09/941,648, co-assigned to the assignee of the present invention, and the entire disclosure of which is hereby incorporated by reference, discloses a system and method for refreshing PCRAM memory cells by applying a positive voltage in the form of a sweep voltage, a pulse voltage, or a step voltage to the cells. The refresh voltages are applied at a magnitude less than that capable of writing a cell to the low resistance state, so that cells in the high resistance state are not affected by the refresh voltages.

BRIEF SUMMARY OF THE INVENTION

[0028] The present invention provides a method for refreshing PCRAM cells and entire arrays of PCRAM cells more efficiently than what is currently being done by using a simple refresh scheme which does not require separate control and application of discrete refresh voltages to the PCRAM cells in an array. In particular, according to the present invention, the PCRAM array structure is constructed to allow PCRAM cells written to the low resistance state to be refreshed by a controlled leakage current to the anode of each cell. In one embodiment, the leakage current flows from the bit lines and across the access device for each cell. In another embodiment, the leakage current flows to the cells through a doped substrate or doped regions of a substrate on which each cell is formed.

[0029] The magnitude of the leakage current through the PCRAM cells is lower than that required to write the PCRAM cells to the low resistance state, but above the baseline current through the cells due to the voltage level maintained at the anode of the cells so as to enable the leakage current to flow continuously across the channel region of the access device or through the substrate, respectively. Accordingly, only those cells in the low resistance state are refreshed by the leakage current, while cells in the high resistance state are unaffected by the refresh operation.

[0030] These and other features and advantages of the invention will be more apparent from the following detailed description, which is provided in connection with the accompanying drawings and illustrate exemplary embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] FIG. 1 is an illustration of a programmable conductor random access memory element as known in the art;

[0032] FIG. 2 is a schematic diagram of a PCRAM cell previously developed in the art;

[0033] FIG. 3 is a structural diagram of a PCRAM cell according to the present invention;

[0034] FIG. 4 is a schematic diagram of an array of PCRAM cells previously developed in the art;

[0035] FIG. 5 shows an exemplary structural diagram of a PCRAM cell in a refresh operation according to a first embodiment of the present invention;

[0036] FIG. 6 illustrates a switch structure for use in the PCRAM cell shown in FIG. 5;

[0037] FIG. 7 shows an exemplary structural diagram of a PCRAM cell in a refresh operation according to a second embodiment of the present invention; and

[0038] Fig. 8 shows a processor system incorporating a memory device having the refresh scheme according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0039] In the following detailed description, reference is made to various specific structural and process embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0040] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a plastic or a semiconductor substrate that has an exposed substrate surface. Semiconductor substrates should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is

made to a substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0041] The term "non-volatile," when used in connection with the described memory device is intended to include any memory device which is generally capable of maintaining its memory state after power is removed from the device for a prolonged period of time (*e.g.*, minutes, days, or weeks), and which may need occasional refreshing to maintain its stored value. As used herein, non-volatile memory devices are also intended to include such memory devices consistent with the foregoing and which are capable of retaining stored data after the power source is disconnected or removed.

[0042] The term "variable resistance material" is intended to include any material usable in programmable conductor memory (PCRAM) elements and/or non-volatile memory elements which exhibit a resistance change in response to an applied stimulus, *e.g.*, a voltage.

[0043] The present invention is applicable in connection with a PCRAM array such as that shown and described above with reference to FIGS. 2 to 4 . However, although FIG. 4 appears to show a separate cell plate for each row of cells 100a-100c and 100d-100f, in the present invention, the cell plate is preferably formed as a common anode to each memory element in the array 200 and is connected to voltage source 112. Also, while the access device 102, as well as the other transistors shown in FIGS. 2 to 4, are depicted as N-type CMOS transistors, it should be understood that P-type CMOS transistors may be used as long as the corresponding polarities of the other components and voltages are modified accordingly. Furthermore, while the present invention is disclosed and described in connection with memory devices having doped chalcogenide glass as the variable resistance material in the programmable conductor

memory elements 104, the invention also encompasses PCRAM devices incorporating any other type of variable resistance memory elements having at least two stable resistive states known to those with ordinary skill in the art, such as the conductive polymer film memory elements, the perovskite memory elements, or the amorphous silicon memory elements disclosed above.

[0044] According to a first exemplary embodiment of the present invention, a refresh operation is simultaneously performed on each memory cell in an array by effecting a leakage current across the access transistor from the memory element. A cross-sectional view of a memory cell 300 in accordance with this exemplary embodiment is shown in FIG. 5. The structure shown in FIG. 5 is very similar to the structure of the memory cell 100 shown in FIG. 3 and discussed above, except that access transistor 102 is replaced with access transistor 302 having a gate 302a, source 302b and drain 302c, and potential source 112 is replaced with potential source 312. While most transistors are produced with the goal of reducing or eliminating current flow across the channel between the source and the drain when the transistor gate is off, transistor 302 in this embodiment is intentionally designed to allow some small current leakage across the channel when the transistor is off.

[0045] In the access transistor 302 according to the present embodiment, the threshold activation voltage V_{GL} is designed to produce a leakage current across the transistor gate 302a when the transistor is off and the drain side 302c is at a potential of 0.2 V relative to the source 302b. For example, this may be accomplished by setting the threshold activation voltage V_{GL} to approximately 0.6-0.7 V, which is a relatively low value and thus renders the transistor particularly susceptible to leakage current. The threshold activation voltage V_{GL} may be determined during the manufacturing process of the access transistor by manipulating any of various factors, including adding a

dopant into the channel region, forming a short channel length, providing a thin oxide layer between the gate and the channel, *inter alia*.

[0046] In a preferred application of the invention, the voltage at potential source 312 and at the bit line 108 are both held at a nominal value of 0.7 V when the memory cell is idle, resulting in 0 V potential difference across the memory cell. Referring now to FIG. 5, the refresh operation is performed by driving the voltage at potential source 312 up to 0.9 V while the bit line is maintained at 0.7 V, to thereby achieve a potential difference of +0.2 V across the channel under the access transistor, which thereby induces a leakage current I_{LT} to flow across the channel. While the exemplary embodiment achieves the leakage current I_{LT} with a potential difference of +0.2 V between the anode 110 and the bit line 108, a potential difference of at least 10% over the baseline voltage 0.7 V and up to a potential difference of about +0.4 V may be safely applied to obtain the leakage current before risking a breakdown of the access transistor 302. For example, in another exemplary embodiment of the invention, the anode is driven up to a voltage of between about 0.79 V and about 0.85 V. Generally, the greater the potential difference across the channel, the greater the leakage current (up to the breakdown voltage of the transistor), and the faster the cells are refreshed. However, it is preferable to keep the leakage current below the voltage level necessary to program the cells. Preferably, the leakage current is maintained as a constant flow through all the memory cells 100 of the array 200 when no access operations (read, write, erase) are being performed on any of the memory cells in the array 200.

[0047] When an access operation is to be performed on a memory cell 300, the access transistor 302 is turned on by applying a voltage V_{GL}, the potential source 312 is switched from the higher voltage level, e.g., 0.9 V, down to the baseline voltage, e.g., 0.7 V, and the voltage of the appropriate bit line 108 is set to an appropriate value to

perform the desired operation. For example, a write operation is performed by setting the bit line to -0.5 V, to thereby obtain a potential difference of +1.2 V across the memory element 104. Similarly, a read operation is performed by setting the bit line to -0.1 V, to thereby obtain a potential difference of +0.8 V across the memory element 104. An erase operation, on the other hand, is performed by raising the voltage of the bit line to +1.7 V, to apply a voltage of -1.0 V across the memory element 104. The voltage at potential source 112 may be selected by means of a switch which alternatively connects to a voltage of +0.7 V or +0.9 V, for example, as shown in FIG. 6.

[0048] For at least PCRAM cells in which the variable resistance material is a doped chalcogenide material, only cells programmed to the low resistance state require refreshing. By producing a low-level leakage current, *e.g.*, in the range of 1-100 picoamps, across the access transistor, the leakage current only flows through the memory cells programmed to the low resistance state. Memory cells which are in the high resistance state are unaffected by this refresh operation because the potential applied to the anode plate of the memory cells is below the threshold level to program these cells to the low resistance state. Moreover, the high resistance across these cells effectively blocks any leakage current from flowing through the cells.

[0049] Although not wishing to be bound by any particular theory, it is believed that the amount of leakage current flowing through the memory element and the transistor channel due to the raised potential at the anode as discussed above serves to reinforce the conductive path(s) between the electrodes and which are present in the low resistance state. It is believed that the leakage current counteracts the natural tendency of the conductive ions in the chalcogenide material to come out of alignment and disperse throughout the chalcogenide material.

[0050] In a second embodiment of the present invention, an array of memory cells is refreshed by a leakage current through the substrate, *i.e.*, current flows from the common anode of the memory elements, through the respective memory elements, and through the substrate on which the memory elements are formed. FIG. 7 shows a cross-sectional view of a memory cell 400 in which a refresh operation is performed by producing a leakage current I_{LS} through the substrate. The structure of memory cell 400 is similar to that of memory cell 100 of FIG. 3 except that the substrate 126 is exchanged for substrate 426, and the p-well region 124 is substituted with p-well region 424.

[0051] In this exemplary embodiment of FIG. 7, leakage current is effected through the substrate by manufacturing the substrate 426 so that the depth "x" of the p-well 424 allows leakage between n-well 122 and the main portion of the substrate 126. Specifically, the p-well 424 is preferably formed to be less than 4000 Å. In contrast, in typical semiconductor structures in which it is desired to reduce leakage through the substrate, the depth of the p-well is formed to be at least 4000-5000 Å.

[0052] With the substrate constructed as described above, leakage current flows through the substrate when a potential difference exists between the common anode 110 and the base of the substrate 426, *i.e.*, ground, up to a breakdown voltage of about 5.5 V. Hence, the presence, absence or amount of a potential difference between the level of the potential source 112 applied to the anode plate 110 and the bit line 108 is not a determining factor in this refresh operation, although leakage current may still occur across the channel under the access transistor simultaneously with the leakage through the substrate. Preferably, however, the level at potential source 112 is operated similarly to the previously described embodiment, in which the potential at the anode of the memory cell is driven to a voltage level in the range of from about 0.79 V to about

0.9 V for the refresh operation, and changed back to 0.7 V for read, write, and erase operations.

[0053] In addition to providing the capability to refresh an entire array of memory cells at one time, the embodiment of refreshing the memory cells by leakage current through the substrate as shown in FIG. 7 offers another advantage in that memory cells not currently being read, written or erased can still be refreshed during the access operation(s) of the other memory cell(s), since the anode of the memory cells is still held at a higher potential than the potential at the base of the substrate during each of the access operations.

[0054] In each embodiment of the invention described herein, PCRAM cells which have been programmed to a low resistance state in an array can be refreshed without disturbing any of the cells in the high resistance state since the high resistance associated with the unprogrammed cells requires an increased the voltage potential across it to cause sufficient leakage current. Thus, no prior knowledge of the states of each of the cells is necessary prior to conducting a refresh operation.

[0055] The present invention allows large memory arrays to be quickly and effectively refreshed by dividing a large array into smaller subarrays with each sub-array sharing a common anode plate. The sub-array anode plates can be driven sequentially to produce leakage current to refresh their respective cells using software or as presented on some hardware driven scheme depending on the rate of refresh desired. In each array or subarray, the p-well may be formed in the substrate in common to all the memory cells in the array, or a separate p-well may be formed in the substrate for each memory cell in the array.

[0056] FIG. 8 illustrates an exemplary processing system 900 incorporating a memory device as describe above in connection with FIGS. 5-7. The processing system 900 includes one or more processors 901 coupled to a local bus 904. A memory controller 902 and a primary bus bridge 903 are also coupled the local bus 904. The processing system 900 may include multiple memory controllers 902 and/or multiple primary bus bridges 903. The memory controller 902 and the primary bus bridge 903 may be integrated as a single device 906.

[0057] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908 which include at least one memory device as described above in connection with FIGS. 5-7. The memory components 908 may be a memory card or a memory module. Examples of memory modules include single inline memory modules (SIMMs) and dual inline memory modules (DIMMs). The memory components 908 may include one or more additional devices 909. For example, in a SIMM or DIMM, the additional device 909 might be a configuration memory, such as a serial presence detect (SPD) memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively, other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller 902 may implement a cache coherency protocol. If the memory controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0058] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, a miscellaneous I/O device 914, a secondary bus bridge 915 communicating with a secondary bus 916, a multimedia processor 918, and a legacy device interface 920. The primary bus bridge 903 may also be coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0059] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be a local area network interface, such as an Ethernet card. The secondary bus bridge 915 may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be a universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to additional devices such as speakers 919. The legacy device interface 920 is used to couple at least one legacy device 921, for example, older styled keyboards and mice, to the processing system 900.

[0060] The processing system 900 illustrated in FIG. 8 is only an exemplary processing system with which the invention may be used. While FIG. 8 illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known

modifications can be made to configure the processing system 900 to become more suitable for use in a variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU 901 coupled to memory components 908 and/or memory arrays 200. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including system based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0061] While the invention has been described in detail in connection with preferred embodiments known at the time, it should be readily understood that the invention is not limited to the disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. For example, although the invention is described in connection with a doped chalcogenide material as the variable resistance material in the memory elements, it should be readily apparent that the present invention is also applicable to other non-volatile or semi-volatile variable resistance memory devices including those incorporating any other type of variable resistance material. Also, the scope and applicability of the present invention not only encompasses the structure of the PCRAM element expressly disclosed herein, but also other variable resistance memory elements including PCRAM elements having different stoichiometric compositions of the disclosed materials, and those having a different number of layered components from that of the disclosed embodiment. Accordingly, the invention is not

limited by the foregoing description or drawings, but is only limited by the scope of the appended claims.